Remarks

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

Disposition of Claims

Claims 1-11 are pending in this application. By way of this reply, claims 1, 10, and 11 have been amended.

Claim Amendments

Claims 1, 5, 10, and 11 have been amended to clarify that the transfer of data and the transfer of the sign bit occur in parallel. No new matter has been added by way of these amendments, as support for these amendments may be found, for example, in Figures 5 and 6 and in paragraphs [0025] and [0032]-[0035] of the present application.

Rejection(s) under 35 U.S.C § 112

Claims 1-11 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. For the reasons set forth below, withdrawal of the rejections is respectfully requested.

Claim 1

Independent claim 1 was rejected as being unclear as to (i) how the bypass is different from the path transferring the data or what is the source and destination of the bypass, (ii) on

what the generation of the sign bit is based, and (iii) what the function of the aligner is with respect to the data transferred.

As shown in Figure 5 of the present application, there are two paths from the SRAM **32** to the aligner **38**. Bypass **50** transfers candidate bits for a sign bit on a different path than the path used to transfer data. Data bits travel first from SRAM **32** to stretcher **140**, which may extend or shrink signals to adjust the timing to transfer data. From stretcher **140**, data is transferred to multiplexer **34**, where a select signal **36** chooses the appropriate data array to be transferred to aligner **38**.

Candidate bits, on the other hand, are routed from SRAM **32**, through bypass **50**, to aligner **38**. From the candidate bits, a sign bit is selected to be transferred to aligner **38**. As shown in Figure 5 of the present application, bypass **50** is a route between SRAM **32** and aligner **38** that is distinct from the route used for data bits. As discussed with reference to Figure 7, candidate bits are selected by obtaining the most significant bits (MSBs) from a given set of data. These groups of MSBs are transferred to sign MUX **52** as candidate bits for the data (*see, e.g.*, Specification, paragraphs [0033]-[0035]). One of the four groups of candidate bits is selected by using a select signal **90** from the select **56**. Operation of select **56** is based on flip-flops **58**. The chosen group of candidate bits is then sent to real-sign MUX **54**. One candidate bit is selected from the group of candidate bits at real-sign MUX **54** based on signal **36** (*see, e.g.*, instant specification, paragraphs [0026]-[0028]).

Aligner **38** receives a real-sign bit from real-sign MUX **54** and data bits from MUX **34**. As seen with reference to Figure 8, aligner **38** may be divided into blocks (**234**, **236**, **238**, and **240**) of sub-aligners (*e.g.*, **230** and **232**). Aligner **38** is a circuit element well known to one skilled in the art. As discussed in paragraph [0005] of the instant specification, aligner **38** transfers data **40** to other elements in a microprocessor. The aligner **38** arranges data in the

appropriate order, and if necessary, may assign an extension according to instructions it receives. In the present invention, aligner **38** may arrange data and assign a unique extension (a sign bit) to the data bits.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 1 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 1 is respectfully requested.

Claims 2 and 6

Claims 2 and 6 were rejected as being unclear as to what the choices of selection are. However, as discussed above, a group of candidate bits is selected as one group from among the four groups of candidate bits by using a select signal **90** from the select **56**, which is controlled by flip-flops **58** (*see, e.g.*, Figure 5; paragraphs [0027]-[0028]). These groups of candidate bits are sent to sign MUX **52** from SRAM **32**. Then, a sign bit is selected from a group of candidate bits at the real-sign MUX **54**. Thus, as required by claim 2 of the present application, a *sign bit* is selected during transfer to the aligner.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claims 2 and 6 are clear and not indefinite. Accordingly, withdrawal of the § 112 rejections of claims 2 and 6 is respectfully requested.

Claims 3, 4, 8, and 10

Claims 3, 4, 8, and 10 were rejected as being ambiguous that the sign bit is generated by selectively processing a part of the data that is transferred from the cache memory to an aligner. However, a sign bit is generated from data that originates in SRAM **32**. As discussed above, candidate bits are selected by obtaining the most significant bits (MSBs) from a given set of data in SRAM **32**. These groups of MSBs are sent to sign MUX **52**, where a group of sign bits is selected to be sent to real-sign MUX **54**. At real-sign MUX **54**, a sign bit is selected to be

sent to aligner **34** (*see, e.g.*, paragraphs [0026]-[0028] of the present application). Thus, it is clear that as only MSBs are selected from all of the data bits to be sent to aligner **38**, a part of the data is used to generate the sign bit, as required by claim 3.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claims 3, 4, 8, and 10 are clear and not indefinite. Accordingly, withdrawal of the § 112 rejections of claims 3, 4, 8, and 10 is respectfully requested.

Claim 5

Independent claim 5 was rejected as being unclear as to (i) how the bypass is different from the path transferring the data or what is the source and destination of the bypass and (ii) what the function of the aligner is with respect to the data transferred.

As discussed previously with reference to claim 1, the bypass is different from the data path in that candidate bits are selectively processed to determine the appropriate sign bit. Additionally, as discussed above, aligner **38** is an element well known to one skilled in the art.

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 5 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 5 is respectfully requested.

Claim 7

Claim 7 was rejected as being unclear as to the inputs and outputs of the multiplexers. However, as discussed above with reference to claim 1, groups of candidate bits are obtained from the most significant bits (MSBs) from a given set of data. In one embodiment of the present invention, four groups of eight MSBs are obtained from four 64-bit data groups (*see, e.g.*, instant specification, paragraphs [0033]-[0035]). These groups of MSBs are transferred to sign MUX **52** as candidate bits for the data. MUX **52**, as seen with respect to Figure 5 of the present application, is controlled by select signal **90**, which originates at select **56**. One of the four

groups of candidate bits is then selected and sent to real-sign MUX **54**. Real-sign MUX **54** is controlled by signal **36**. One candidate bit is selected from the group of candidate bits at real-sign MUX **54,** based on signal **36** (*see, e.g.*, instant specification, paragraph [0028]).

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 7 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 7 is respectfully requested.

Claim 11

Independent claim 11 was rejected as (i) being ambiguous that the sign bit is generated by selectively processing a part of the data that is transferred from the cache memory to an aligner and as (ii) being unclear as to what the inputs and outputs of the multiplexers are. However, as discussed above with reference to claims 3 and 7, candidate bits are selected by obtaining the most significant bits (MSBs) from a given set of data. These groups of MSBs are sent to sign MUX **52**, where one group of sign bits is selected to be sent to real-sign MUX **54**. At real-sign MUX **54**, a sign bit is selected to be sent to aligner **34**. Thus, it is clear that as only MSBs are selected from all of the data bits to be sent to aligner **38**, a part of the data is used to generate the sign bit.

Additionally, as discussed above with reference to claim 7, groups of candidate bits are obtained from the most significant bits (MSBs) from a given set of data. In one embodiment of the present invention, four groups of eight MSBs are obtained from four 64-bit data groups (*see, e.g.*, instant specification, paragraphs [0033]-[0035]). These groups of MSBs are transferred to sign MUX **52** as candidate bits for the data. One of the four groups of candidate bits is then sent to real-sign MUX **54**. One candidate bit is selected from the group of candidate bits at real-sign MUX **54** based on signal **36** (*see, e.g.*, instant specification, paragraphs [0028]).

Thus, with respect to the Examiner's rejections under 35 U.S.C. § 112, second paragraph, claim 11 is clear and not indefinite. Accordingly, withdrawal of the § 112 rejection of claim 11 is respectfully requested.

Rejection(s) under 35 U.S.C § 102

Claims 1-11 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,638,312 issued to Simone (hereinafter "Simone"). By way of this reply, independent claims 1, 5, 10, and 11 have been amended to clarify the present invention. To the extent that this rejection may still apply to the amended claims, this rejection is respectfully traversed.

The present invention is directed to a method and apparatus for reducing signed load latency in a microprocessor. As shown in Figure 5 of the present application, embodiments of the present invention may include a bypass **50** to transfer candidate bits, which include a sign bit, to an aligner **38**. Data bits are selectively arranged and transferred along the bypass **50** to obtain the candidate bits (*see* paragraph [0025] of the instant specification). Data from SRAM **32** follows a data path to stretcher **140**, where the data is shrunk or extended for timing purposes. From the stretcher data continues to multiplexer **34**, where part of the data is chosen and transferred to aligner **38**.

Accordingly, amended independent claim 1 of the present invention requires (i) transferring data from a the cache memory to an aligner, (ii) generating a sign bit for the data, and (iii) transferring the sign bit to the aligner via a bypass, where transferring data and transferring the sign bit occur in parallel.

On the other hand, Simone is directed to a method and apparatus for generating a zero flag (z-flag) status signal in a microprocessor. As seen in Figure 6 of Simone, a load aligner **102**

contains a multiplexer controller **601** and a multiplexer circuit **602**. Data signals are inputted directly to multiplexer **602**. Signals **M1-M7** are control signals that are transferred from multiplexer controller **601** to multiplexer circuit **602** (*see* Simone, col. 8, lines 5-8). As seen in Figure 7 of Simone, multiplexer circuit **602** contains multiplexers **701-707**.

Further, as seen with reference to Figures 1 and 2 of Simone, unsigned data are inputted directly to the load aligner **102**. As all information regarding the data bits and sign bits is processed *in* the load aligner, it is impossible for the device of Simone to transfer the sign bit *to* the aligner via a bypass, as required by amended independent claim 1 of the present application.

Further, Simone clearly states that load alignment **808** includes the steps of ***first*** reordering **803** the data bits and ***then*** sign extending **809** the most significant bit to form a word (*see* Simone col. 11, lines 40-42). As shown in Figure 8 of Simone, it is clear that these processes are sequential. Simone does *not* teach transferring the sign bit to the aligner via a bypass, where the transferring of the sign bit is parallel to the transferring of the data as required by the claimed invention. In fact, by teaching that sign extension occurs sequentially after the data bits are reordered, Simone in no way even inherently teaches the "parallel" limitations of the claimed invention.

Accordingly, Simone fails to disclose, or otherwise teach, reducing signed load latency in transfer of data from a cache memory to another element in a microprocessor by (i) transferring data from a the cache memory to an aligner, (ii) generating a sign bit for the data, and (iii) transferring the sign bit to the aligner via a bypass, wherein transferring the sign bit is parallel to transferring data as required by independent claim 1 of the present application. In view of the above, Simone fails to show or suggest the present invention as recited in independent claims 1, 5, 10, and 11 of the present application. Thus, independent claims 1, 5, 10,

and 11 are patentable over Simone. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.

Conclusion

Applicant believes this reply is fully responsive to all outstanding issues and places the present application in condition for allowance. If this belief is incorrect, or other issues arise, the Examiner is encouraged to contact the undersigned or his associates at the telephone number listed below. Please apply any charges not covered, or any credits, to Deposit Account 50-0591 (Reference Number 03226/035001; P5030).

Dated: December 6, 2004

Respectfully submitted,

By W Kussler REG. NO. 51,048

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